UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,366	02/01/2001	Tongbi Jiang	303.706US1	8118

7590 11/27/2002

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Danny J. Padys
P.O. Box 2938
Minneapolis, MN 55402

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applic	
09/755,366	Jiang et al	
Examiner	Art Unit	
Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 10, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-52, 108-126, 136-154, and 252-269* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-52, 108-126, 136-154, and 252-269* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 1
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-52, 108-126, 136-154 and 252-269 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Yamamoto et al (US Pat. 6265782), Penry (US Pat. 6049094), Satsu et al (US Pat. 6225418) and Narita (US Pat. 6144107).

Regarding claims 1, 3 and 7, the APA discloses an integrated circuit (IC) package comprising:

- a substrate comprising conventional plastic/board/PCB, ceramic, glass, glass-epoxide, etc.
- a die, and
- a material having a low Young's modulus (YM) at a conventional/solder reflow temperature attaching the die to the substrate

(Fig. 1A/B; specification pp. 1-3).

The APA fails to specify using:

a) the die comprising one or more memory, processor, logic, communication or application specific Ics, and

b) the material having YM value between 0.1-20 megapascals (Mpa) and a Shore A/D hardness of greater than 70/20 respectively or coefficient of thermal expansion (CTE) of less than 400 ppm/deg. C, and

- the material comprising polyepoxide formed from one or two epoxides, polyacrylate, polyolefin, polyimide, a mixture of at least two of the above components or a copolymer of at least two of the above components.

a) It is conventional in chip packaging and interconnection technology art to use IC die comprising memory, logic, optical sensor, flash memory, bipolar, processor, hybrid circuits to provide a variety of functions such as large scale integration (LSI), chip/circuit density, I/O connections per unit, speed, performance, etc. The cited references (Narita and Penry) teach using a die/IC comprising an application specific/solid state charge coupled device or any other type of CMOS chip (Col. 1, line 18; Col. 8, line 10) and CMOS based transistors in a liquid crystal display application (Col. 1, line 20) respectively.

b) Yamamoto et al teach using an adhesive/die-attach material (1/3 in Fig. 1-8) comprising a variety of conventional resin/polymer based materials which include a component and a mixture/copolymer thereof including epoxy, phenol, bisphenol, acrylate, polyimide, polyether-imide, etc. providing the desired properties such as elasticity/modulus, strength, tackiness, surface hardness, heat dissipation, etc (Col. 4-21).

Yamamoto et al further teach using a variety of compositions/formulations of such adhesives having YM value between 1-50 Mpa (Col. 3, line 34; examples in Tables 2 and 3; Col. 3-32) and having a wide range of molecular weight providing thermoplastic or thermosetting/rigid properties.

Penry teaches using conventional die attach material having Shore D hardness of about 80 (Col. 4, line 48).

Narita teaches using an adhesive material having Shore D hardness between 20-30 (Col. 6, line 38).

Satsu et al teaches using a variety of resin compositions for die attach/encapsulation (Fig. 4A/B; Col. 3-24) having a CTE values being less than 400 ppm/deg. C (Tables 1-3).

Furthermore, the determination of parameters and respective values/ranges such as YM, hardness, viscosity, thermal expansion coefficient (TEC), etc. of various die attach material/encapsulant and respective composition/formulation in chip

packaging/encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, mechanical and electrical properties for the IC package.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at the values/ranges as cited in elements a) -c) so that the defects related to elasticity/modulus and thermal expansion can be reduced and tackiness/adhesion can be improved using Yamamoto et al, Penry and Narita's die attach material/composition in the APA structure.

Regarding claims 2, 4-6 and 8-52, the claim elements have been addressed in the rejection as explained above for claims 1, 3 and 7.

Regarding claims 108-126, as explained above for claims 1-52, the APA discloses using a ceramic/ceramics substrate but fails to specify using a single or multimetal layer ceramic (MLC).

It is conventional in the chip packaging technology and fabrication art to use substrates/boards made of plastic, ceramic, etc. in the form of multilayer structure.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a single or multimetal layer ceramic to

improve the thermal and mechanical properties using Yamamoto et al, Penry and Narita's die attach material in the APA.

Regarding claims 136-154, the claim elements have been addressed in the rejections as explained above for claims 108-126 and 1-17.

Regarding claims 252-269, the claim elements have been addressed in the rejection as explained above for claims 1-17.

Response to Arguments

3. Applicant's arguments filed on 09-10-02 have been fully considered but they are not persuasive.

A. Applicant contends that using the cited references/admitted prior art is not a prior art and the rejections are improper.

However, as explained above, the conventional IC package comprising the substrate, die, and the material having a low Young's modulus is disclosed in the prior art/APA as cited in the pages 1-3 of specification and Fig. 1A/B.

The prior art teachings of Yamamoto et al, Penry, Satsu et al and Narita is applied to the APA to achieve the claimed ranges/values for the die attach material

parameters including modulus, CTE and hardness. Furthermore, the determination of such parameters and arriving at a desired range of YM, hardness, viscosity, TEC, etc. of a die attach material having different composition in chip packaging/encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, mechanical and electrical properties for the IC package.

B. Applicant contends that Yamamoto et al teach away from using a rigid die attach material.

However, as explained above, Yamamoto et al teach using a variety of adhesives/die-attach material (1/3 in Fig. 1-8) comprising conventional resin/polymer based materials/component and a mixture/copolymer thereof including epoxy, phenol, bisphenol, acrylate, polyimide, polyether-imide, etc. having a wide range of molecular weight after curing providing the desired thermosetting/rigid properties, strength, tackiness, surface hardness, heat dissipation, etc (Col. 8, line 5-65; Col. 4-21; Col. 3, line 34; examples in Tables 2 and 3; Col. 3-32). Yamamoto et al further teach solving the problems encountered by the conventional adhesive films having low rigidity by using a variety of epoxy/acrylic/polyimide formulations having a thermosetting/rigid properties in a cured/final stage (Col. 18, line 32- Col. 20, line 58).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

11-22-02

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800